Characterization and Testing of CMOS Subcircuits in a Mixed Signal IC

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Abstract

In a response to today's trend in technology, the theoretical focus of most digital and analog based circuit courses is shifting towards CMOS technology. Due to the lack of proper laboratory testing circuits and environments for CMOS technology; older, obsolete circuits are used in many laboratory classes. While these labs afford students the chance to compare classroom analysis to real laboratory results, they fail to provide an accurate portrayal of today's technology. In an attempt to combat this problem, Dr. James Morizio designed a chip to provide CMOS devices that could be used in an introductory laboratory class. The purpose of this independent study was to design a test fixture that would allow the chips to be tested, to design test circuits that would allow the devices to be tested, to test the functionality of the devices in the laboratory and to compare the laboratory results to HSPICE simulation results, and finally to rewrite the labs for ECE163 using the CMOS devices. The test fixture that allowed all of the devices to be tested was built by Jennifer Wilbur and Jessica Smith. The circuit designs were a collaborative work between Jessica Smith, Jennifer Wilbur, Dr. James Morizio, and Dr. Jeffrey Derby. Laboratory measurements were led by Jennifer Wilbur, while HSPICE simulations were led by Jessica Smith. The circuits tested were the individual NMOS and PMOS devices, the inverter, the current mirror, the common source amplifier, the source follower, the differential pair, and the two stage operational amplifier. Some devices, such as the individual devices and the inverter, yielded similar simulated and experimental results. Other results such as those on the op amp, source follower, and common source amplifier were not as similar but still matched fairly well. For the current mirror and the differential pair no valid experimental results were obtained, as the devices did not work. The end conclusion of this study is that the test CMOS device is neither stable nor reliable enough to be used in the laboratory at this point.

Introduction

Currently, the electrical engineering program at Duke University relies heavily upon the use of BJT's in the laboratory as they allow for a fairly simple construction of basic circuits. While BJT's are no longer a significant focus in the "real world", they continue to receive a disproportionate focus in the classroom as they are currently the only devices allowing students to have the experience of both analyzing and then running tests on circuits. This laboratory focus upon BJT's permits less time to be spent on the more dominant CMOS technology. CMOS devices are not as easy to use in lab because of their requirement of being perfectly matched in order to correctly function in circuits. Duke's Electrical Engineering program searched for solutions to this problem but determined that this is a nationwide problem and that no pre-fabricated devices existed that solved this problem.

The chip used in this study was designed by Dr. James Morizio after he collected feedback from Doug Holberg (University of Texas), Dr. Martin Brooke (Georgia Tech), Dr. Bill Richards (Thunderbird Technologies), and Dr. Jeff Derby (IBM) on which devices should be on the circuit. The chip that was designed contains a mix of electronics from beginner Complimentary Metal Oxide (CMOS) circuits to advanced Operational Transconductance Amplifiers (OTA) circuits. Mentor Graphics DA and IC were used to create the device's design and layout. The chip was fabricated using a 0.5µm double poly, triple level metal, 5V CMOS process from AMI Semiconductor Corp. The device was packaged in an 84 pin PGA ceramic package by Promex Industries, Inc. Five devices were packaged and made available for testing in this study.

The goals of this study were to design a test fixture that would allow the chips to be tested, to design test circuits that would allow the devices to be tested, to compare the results from simulations using HSPICE and results found in the laboratory, and to produce a revised laboratory manual for ECE163 that could be used in the Fall of 2005 using the CMOS devices on the chip.

The paper begins with a description of general testing methods and then summarizes the tests run on the individual subcircuits. It then reviews the results from both the simulation and laboratory tests for each subcircuit. Finally, the results for each device are analyzed and the problems encountered during this study are examined in the discussion.

Procedure and Test Data

Simulation and Test Methodology

Simulation Extraction method
The individual devices were isolated into their own file using Mentor Graphics IC. They were then checked to make sure that they were DRC and LVS clean. Next, ICextract (M) was selected and the distributed option was used to produce a netlist that accounted for the capacitances and resistances present. This generated a spice_out file and a .pex file that were used for the simulation tests on each device. The HSPICE level used by the rules file was level 49.

Chip Description
Dr. James Morizio designed and produced the chip layout using Mentor Graphics tools. The chip was fabricated by AMI Semiconductor Corporation using a 0.5µm double poly, triple level metal, 5V CMOS process. The five chips used for testing were packaged in a 84 pin PGA84M ceramic package by Promex Industries, Inc.. This is a 1.1" square package. The pins of the packages were arranged on an 11 x 11 pin grid at 0.1" centers.

Subcircuits on the chip
Tested Subcircuits: Two NMOS devices, Two PMOS devices, Inverter, Current Mirror, Common Source Amplifier, Source Follower, Differential Pair, and Two Stage Operational Amplifier.
Other Subcircuits: Current Mirror Amplifier, Two Stage Cascode, Two Stage Fully Differential Cascode, Rail-Rail Amplifier, Cascode Current Mirror, Fixed Taper, and Variable Taper.

Construction of Test Fixture
The test fixture was built on a 4"x 5" Twin Industries board with 0.037" plated holes. A 13x13 Aries 0.1" socket was soldered on and used to test the various chips. Square test pins were soldered into the board and then connected to the underside of the socket using 30 gauge wire that was then soldered to the underside of the socket and wire wrapped to the test pins. All of the grounds on the chip were tied together and connected to a jack.

Laboratory Equipment
The laboratory equipment used was: the Agilent 34401A Multimeter, the Agilent E3631A DC Power Supply, the Agilent 33220A Function Generator, the Agilent 54624A Oscilloscope, and the HP 3577B Network Analyzer.

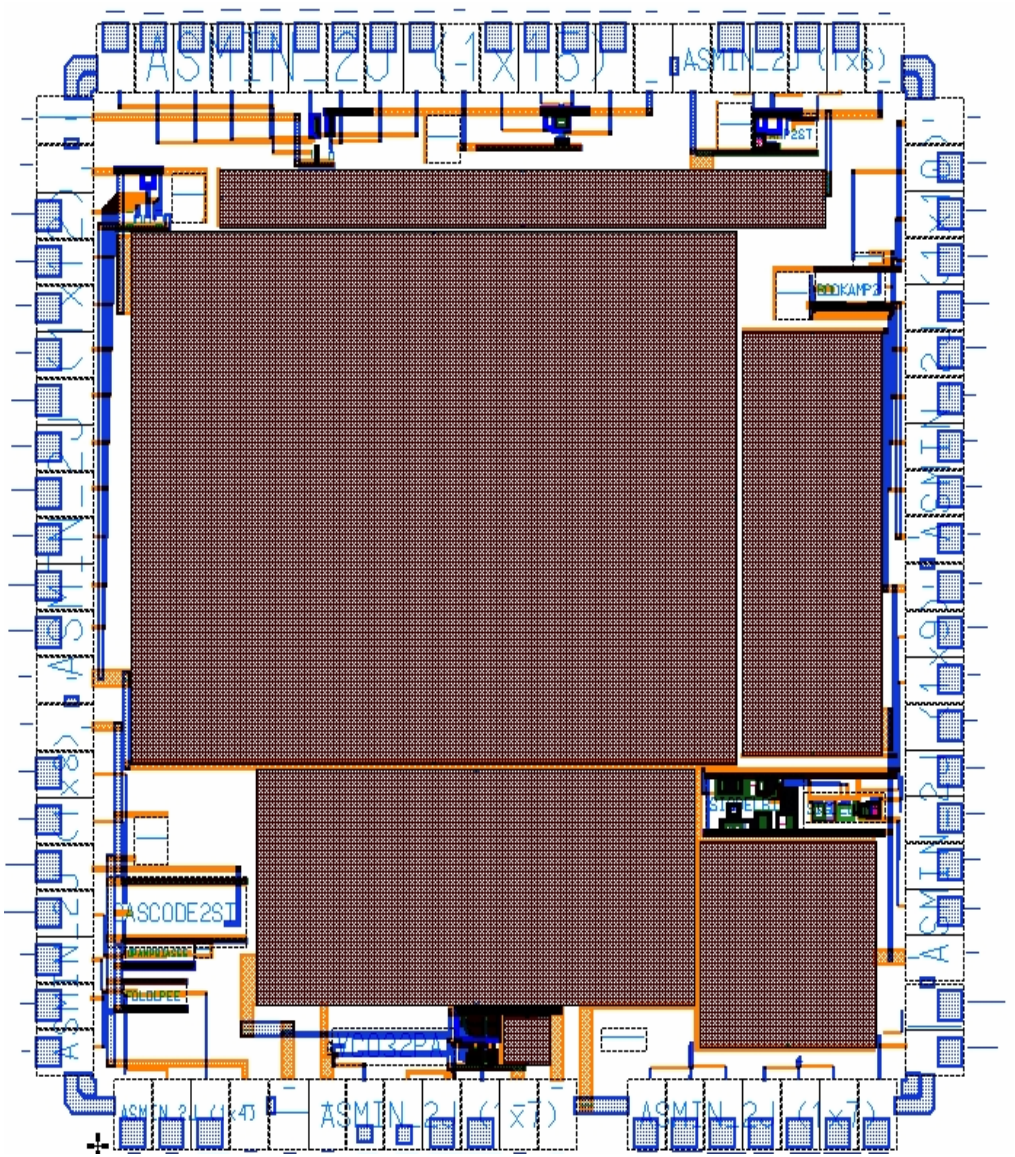

Figure 1: Chip Layout

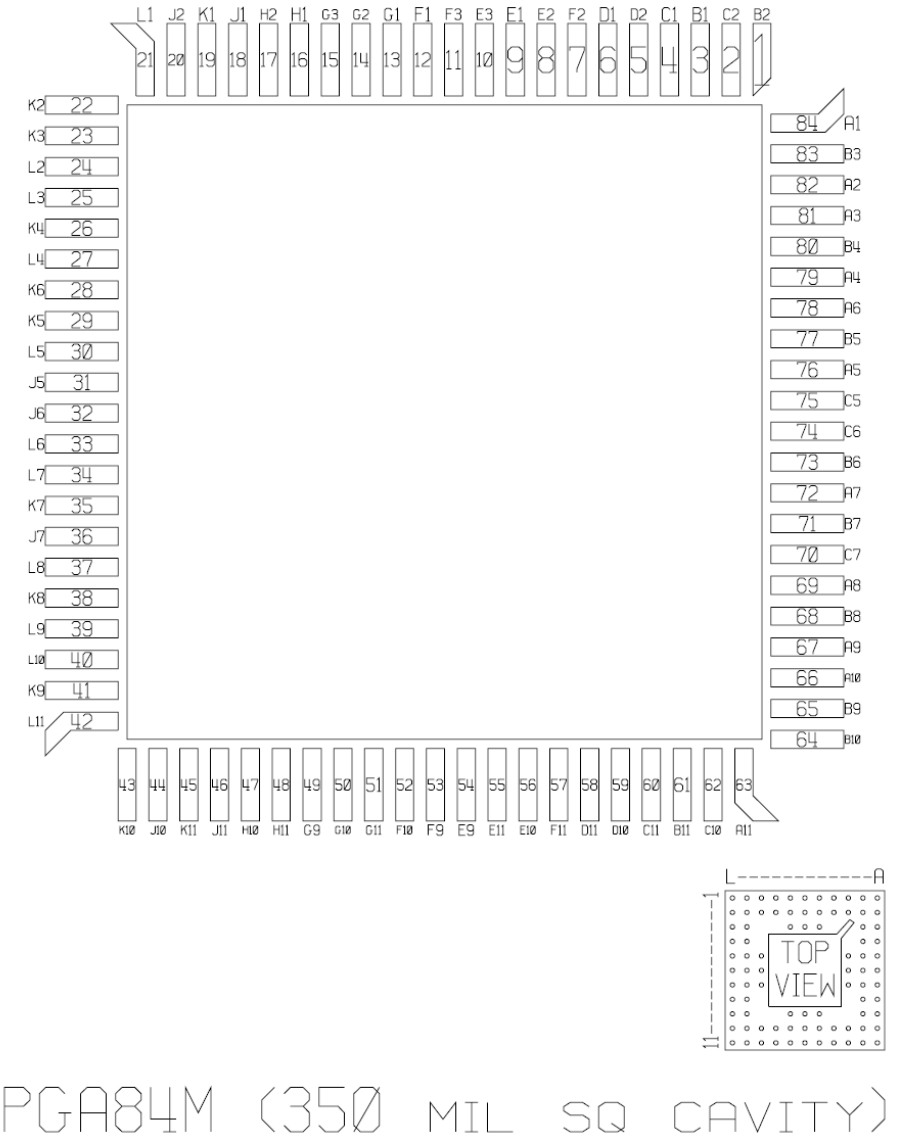

Figure 2: Package Pin Out Diagram

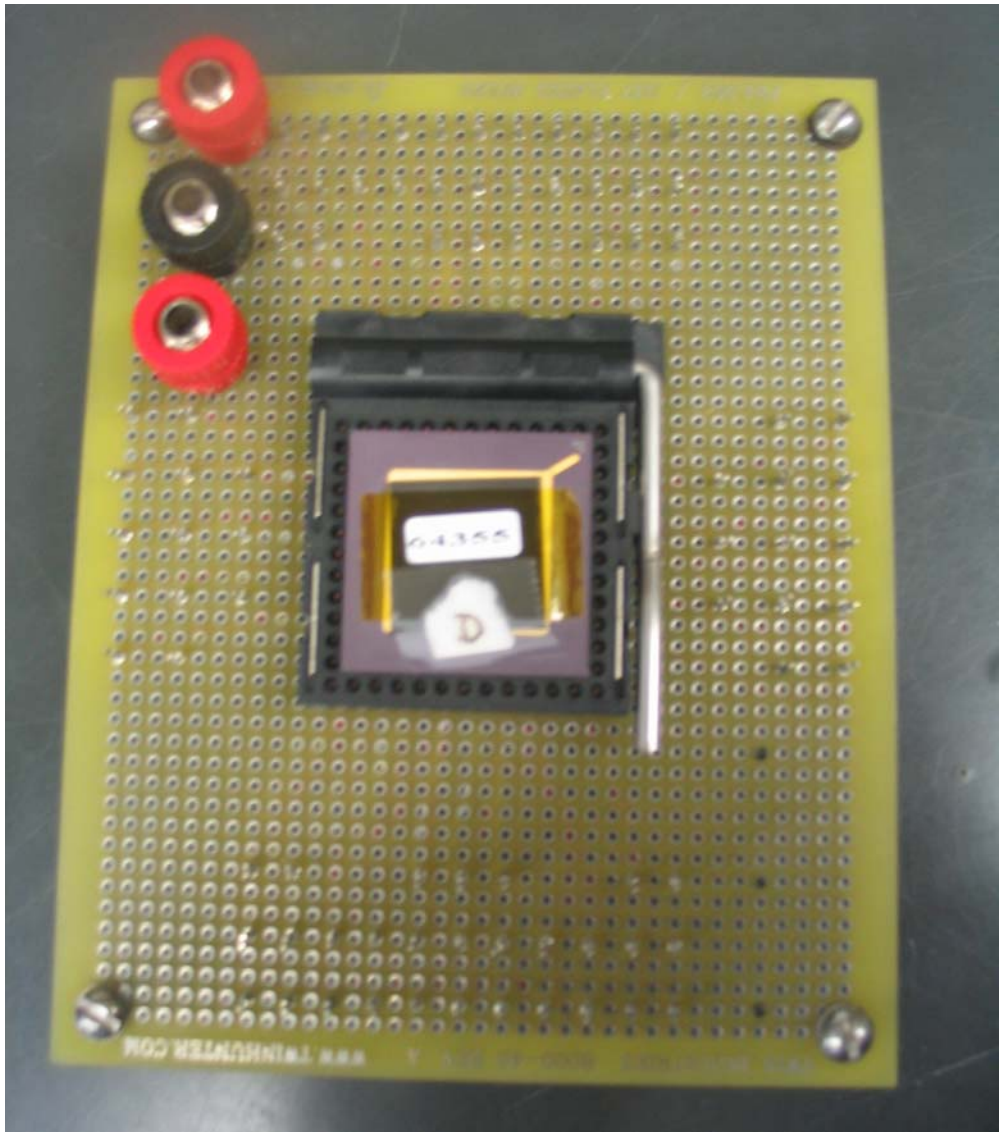

Figure 3:Top Side of the Test Board

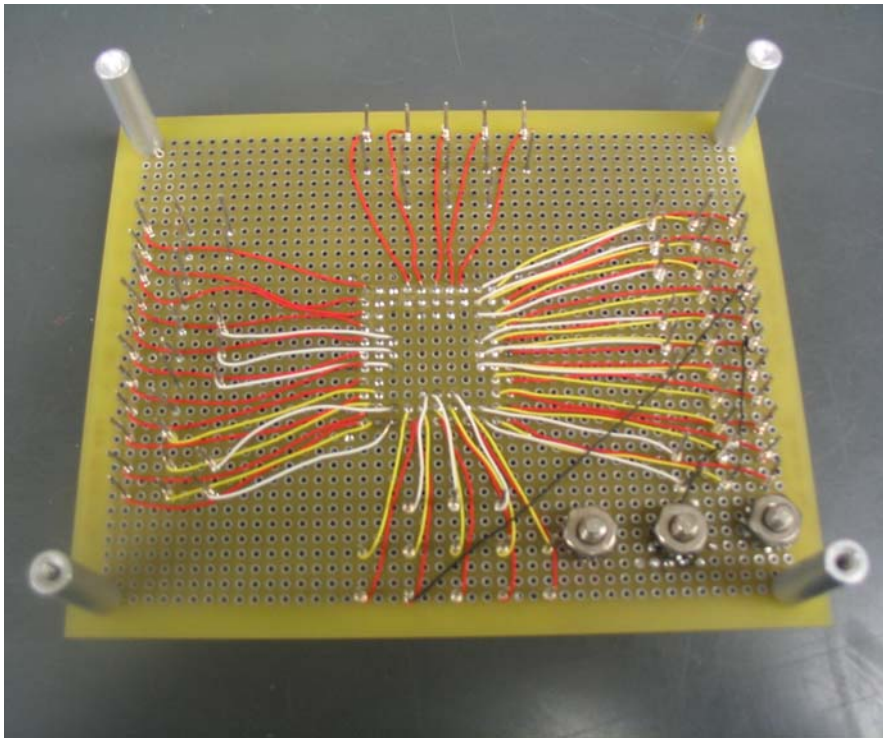

Figure 4: Underside of the Test Board

Device Layouts, Testing Circuits and Testing Methods

All of the devices and circuits were tested in the laboratory and were simulated using HSPICE. In the laboratory the tests were run on all five chips. Labview was used to perform many of the sweeps in the laboratory. The pin outs in the tables in this section refer to the pin out diagram in Figure 2.

PMOS

The PMOS devices, PMOS1 and PMOS2, are shown in Figure 5. The pin outs for the PMOS devices are shown in Table 1.

HSPICE Simulation and Laboratory Testing: VDS was swept from 0V to -5V for VGS set to 0, -1, -2, -3, -4, and -5V and the drain current (ID) was measured. VGS was swept from 0V to -5V with VDS held constant at -5V. These conditions were tested on both PMOS1 and PMOS 2 using outp1 and outp2 respectively.

NMOS

The NMOS devices, NMOS1 and NMOS2, are shown in Figure 5. The pin outs for the NMOS devices are shown in Table 1.

HSPICE Simulation and Laboratory Testing: VDS was swept from 0V to 5V for VGS set to 0, 1, 2, 3, 4, and 5V and the drain current (ID) was measured. VGS was swept from 0V to 5V with VDS held constant at 5V. These conditions were tested on both NMOS1 and NMOS 2 using outn1 and outn2 respectively.

Inverter

The Inverter design is shown in Figure 6. The pin outs for the Inverter are in Table 2.

HSPICE Simulation and Laboratory Testing: INV IN was swept from 0V to 5V and the voltage was measured at INV OUT.

Current Mirror

The Current Mirror design and testing circuit is shown in Figure 6. The pin outs for the Current Mirror are in Table 2.

HSPICE Simulation: The circuit in Figure 7 was set up with R2 at 10Ω and R1 swept from 100 Ω to 1k Ω and the voltages across the resistors were measured.
Laboratory Testing: The circuit in Figure 7 was set up with R1=R2=10k Ω and the voltages across the resistors were measured.

Common Source Amplifier

The design of the Common Source Amplifier as well as the testing circuit used for both the DC and AC testing are shown in Figure 8. The pin outs for the Common Source Amplifier are in Table 4.

HSPICE Simulation: The circuit in Figure 8 was set up with the given values and a capacitor of 10pF was connected from CSOUT to GND in order to simulate the

capacitance in the oscilloscope probes used in lab. A DC sweep on CSIN was performed from 0 to 5V. An AC sweep was performed using the network analyzer to find the gain and 3dB frequency of the circuit.
Laboratory Testing: The circuit in Figure 8 was set up and the same DC and AC tests were performed that were performed in HSPICE simulation.

Source Follower
The design of the Source Follower as well as the testing circuit used for both the DC and AC testing are shown in Figure 9. The pin outs for the Source Follower are in Table 5.

HSPICE Simulation: The circuit in Figure 9 was set up with the given values and a 10 pF capacitor was connected from SFOUT to GND in order to simulate the capacitance in the oscilloscope probes used in lab. A DC sweep on SFIN was performed from 0 to 5V. An AC sweep was performed using the network analyzer to find the gain and 3dB frequency of the circuit.
Laboratory Testing: The circuit in Figure 9 was set up and the same DC and AC tests were performed that were performed in HSPICE simulation.

Differential Pair
The design of the Differential Pair as well as the testing circuit used for both the DC and AC testing are shown in Figure 10. The pin outs for the Differential Pair are in Table 6.

HSPICE Simulation: The circuit in Figure 10 was set up with the given values and a 10 pF capacitor was connected from DIFFOUT1 to GND to simulate the capacitance in the oscilloscope probes used in lab. A DC sweep on INNEG1 was performed from 0 to 5V with INPOS1=2.5V. Then a DC sweep on INPOS1 was performed from 0 to 5V with INNEG1=2.5V. An AC sweep was then performed using the network analyzer to find the gain and 3dB frequency of the circuit.
Laboratory Testing: The circuit in Figure 10 was set up and the same DC and AC tests were performed that were performed in HSPICE simulation.

Two Stage Operational Amplifier
The design of the two stage operational amplifier is shown in Figure 11. The testing circuit used for the AC analysis is shown in Figure 12 and the circuit used for the DC analysis is shown in Figure 13. In both of these Figures the OPAMP symbol is used to represent the two stage operational amplifier from Figure 11. The pin outs for the operational amplifier are in Table 7.

HSPICE Simulation: In the simulation a10 pF capacitor was connected from OPOUT to GND to simulate the capacitance in the oscilloscope probes that are used in lab. A 10 pF capacitor was connected from OPOUT to GND to simulate the capacitance in the probes that must be used in lab.
Laboratory Testing: The circuit in Figure 13 was set up with the given values. A DC sweep was performed on OPINPOS from 0 to 5V with OPINNEG held constant at 2.5V. Then Figure 12 was set up and an AC sweep was then performed using the network analyzer to find the gain and 3dB frequency of the circuit.

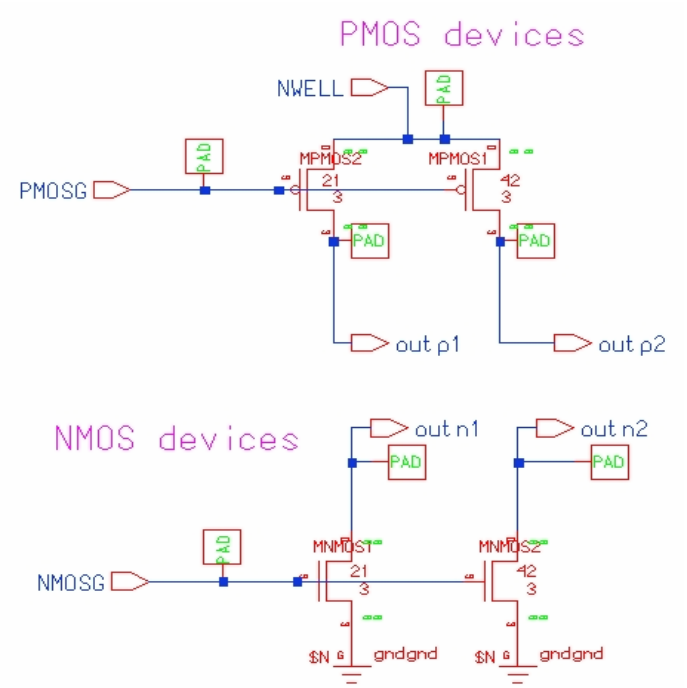

Figure 5: PMOS and NMOS Design

Name	Pin
PMOSG(G)	H2
NWELL(S)	G1
outp1(D)	J2
outp2(D)	J1
NMOSG(G)	J2
outn1(D)	L1
outn2(D)	K1
VDD	F2
GND	F1

Table **1**:PMOS and NMOS pin outs

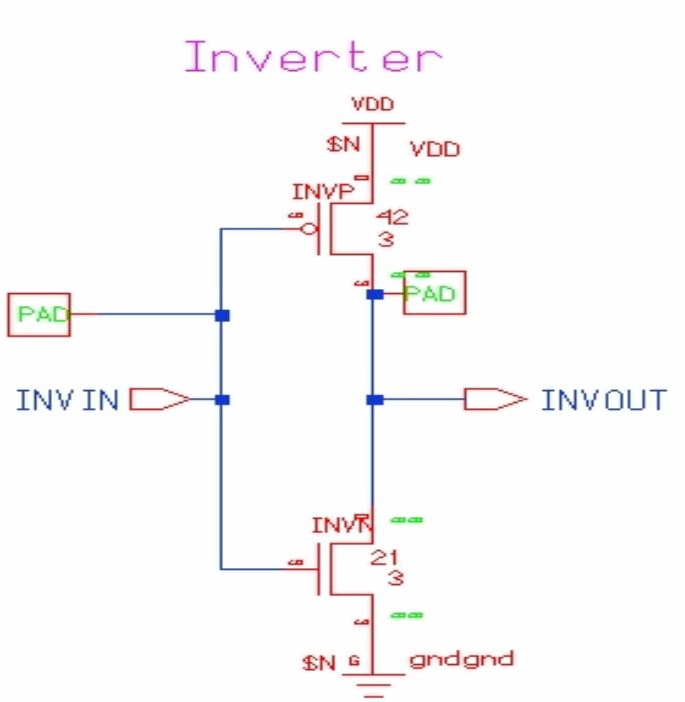

Figure 6:Inverter Design

Name	Pin
INV IN	G2
INV OUT	G3
VDD	F2
GND	K2

Table 2: Inverter pin outs

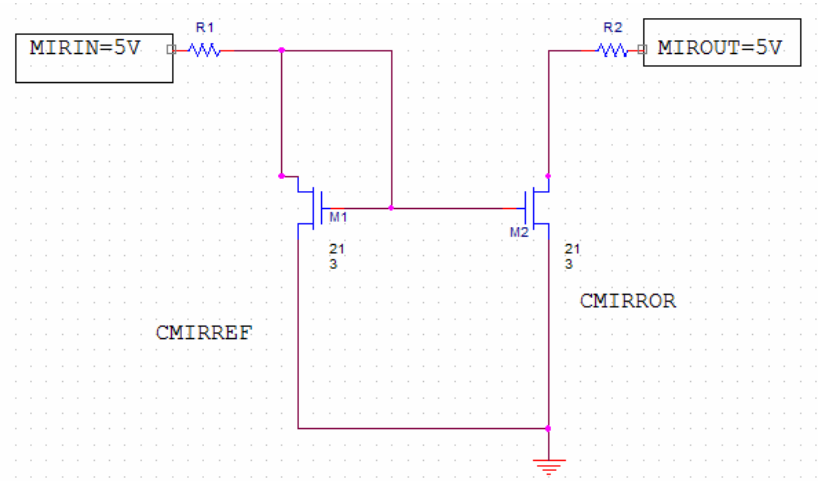

Figure 7: Current Mirror Diagram

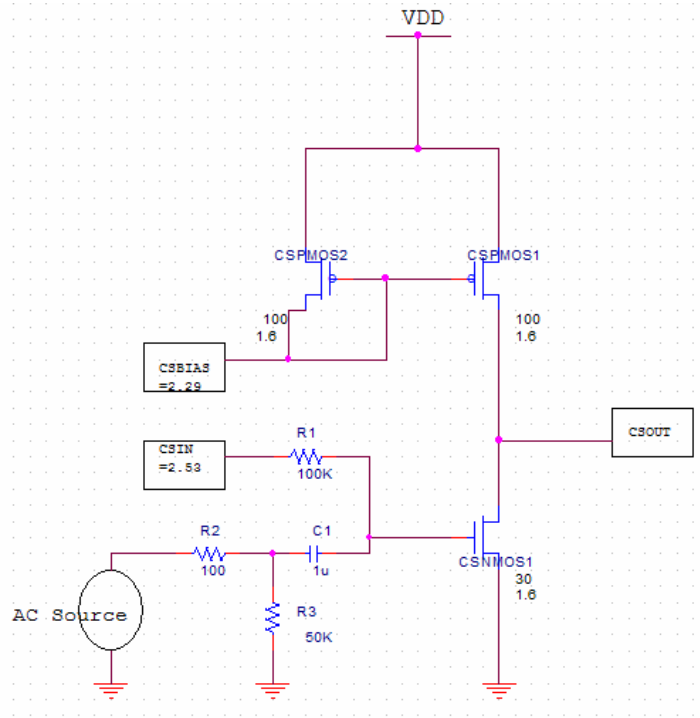

Figure 8:Common Source Amplifier Diagram

Name	Pin
MIR IN	J5
MIR OUT	L5
VDD	K7
GND	L7

Table 3:Current Mirror Pin Out

Name	Pin
CSIN	K4
CSBIAS	L2
CSOUT	L3
VDD	K3
GND	L7

Table 4:Common Source Pin Out

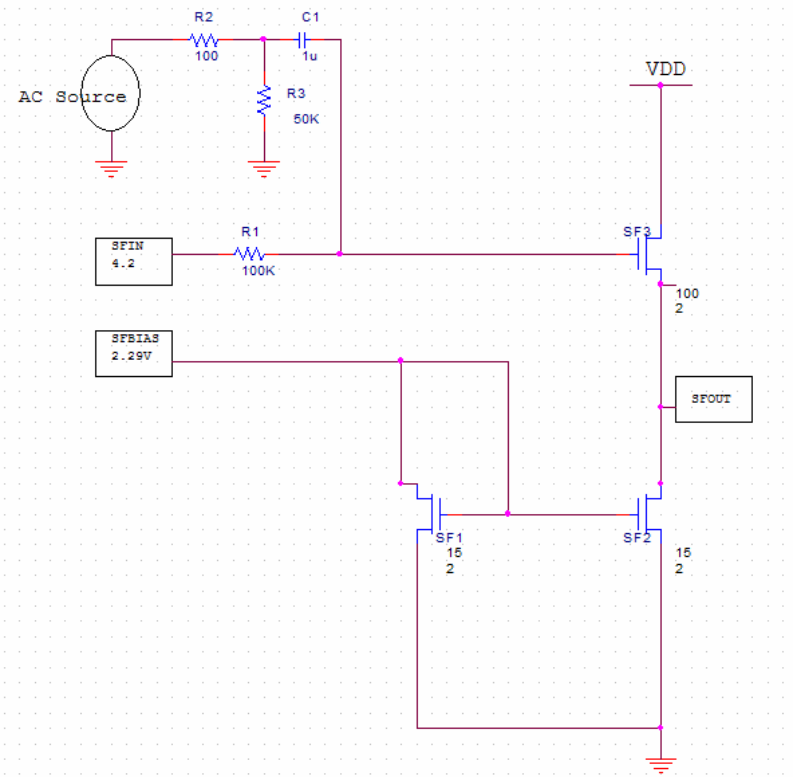

Figure 9: Source Follower Diagram

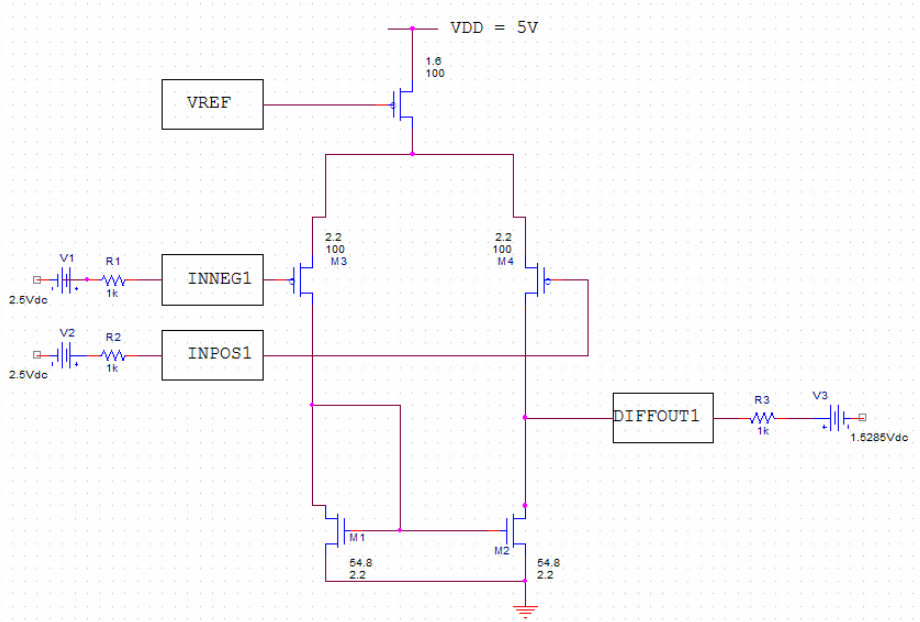

Figure 10: Differential Pair Diagram

Name	Pin
SFIN	L4
SFBIAS	K6
SFOUT	K5
VDD	K7
GND	L7

Table 5: Source Follower Pin Out

Name	Pin
INNEG1	E3
INPOS1	E1
VREF	F3
DIFFOUT1	E2
VDD	F2
GND	F1

Table 6: Differential Pair Pin Out

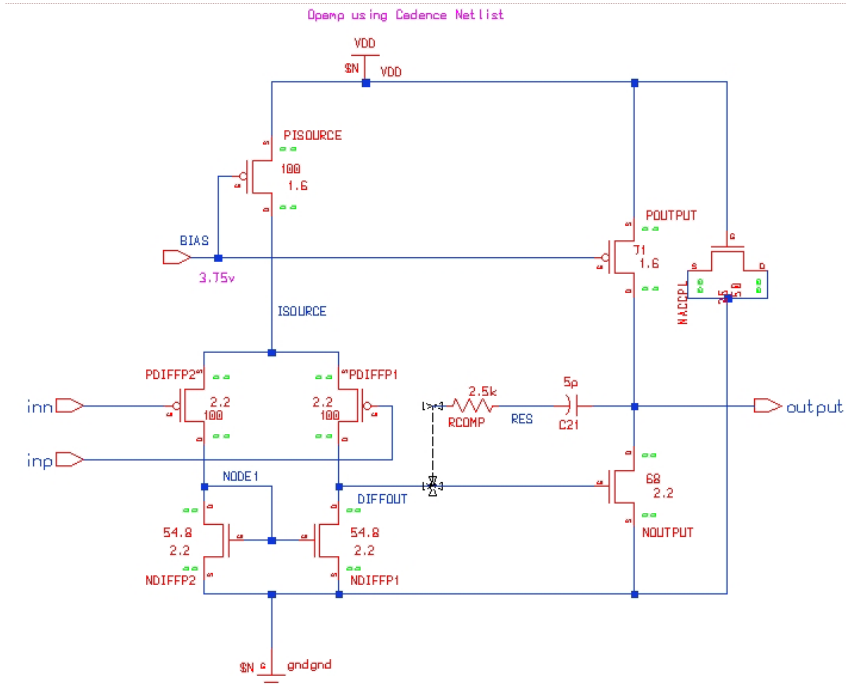

Figure 11: Two Stage Op Amp

Name	Pin
OPINPOS	B1
OPINNEG	C1
OPBIAS	D2
OPOUT	C2
VDD	B2
GND	D1

Table 7: Two Stage Op Amp

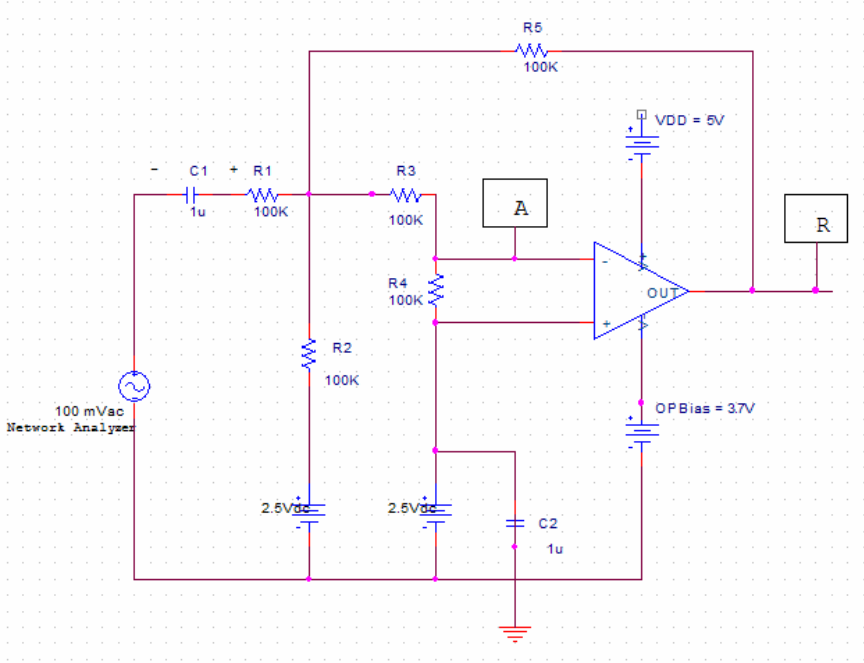

Figure 12: Two Stage Op Amp (AC Analysis)

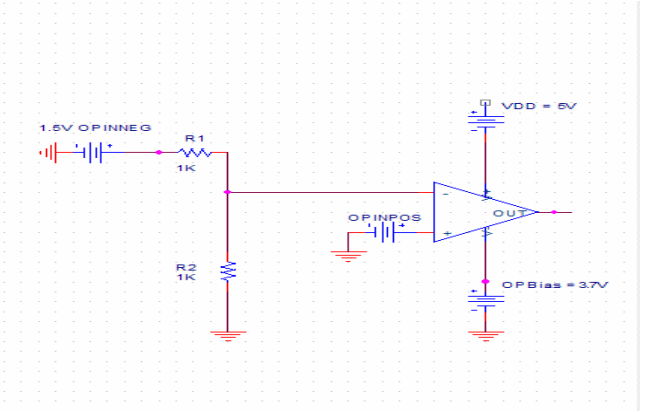

Figure 13: Two Stage Op Amp (DC Analysis)

Results

PMOS Devices
All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (A and D) that produced valid results. Figure 14 is the plot of PMOS1 ID vs. VDS. Figure 15 is the plot of PMOS1 ID vs. VGS. Figure 16 is the plot of PMOS2 ID vs. VDS. Figure 17 is the plot of PMOS2 ID vs. VGS.

NMOS Devices
All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (A and D) that produced valid results. Figure 18 is the plot of NMOS1 ID vs. VDS. Figure 19 is the plot of NMOS 1 ID vs. VGS. Figure 20 is the plot of NMOS2 ID vs. VDS. Figure 21 is the plot of NMOS2 ID vs. VGS.

Inverter
All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (A and D) that produced valid results. Figure 22 is the plot of VIN vs. VOUT.

Current Mirror
None of the chips tested produced valid results in the laboratory. Although there was a small measured voltage drop across R1 as shown in Figure 7, there was no voltage drop across R2. The results from HSPICE when a sweep of R1 was performed are plotted in Figure 23.

Common Source Amplifier
All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (B and D) that produced valid results. The DC plot of CSIN vs. CSOUT is in Figure 24 and the AC gain plot is in Figure 25. The 3dB frequencies and max gains are shown in Table 8**.**

Table 8: Common Source Amplifier Gain and 3dB Results

	HSPICE	Chip B	Chip D
Max Gain (dB)	25	23.61	23.78
%Diff from HSPICE	-	5.56	4.88
3dB Frequency (MHz)	1.79	.762	.696
%Diff from HSPICE	-	57.4	61.1

Source Follower
All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (A and D) that produced valid results. The DC plot of SFIN vs. SFOUT is in Figure 26 and the AC gain plot is in Figure 27. The 3dB frequencies and max gains are shown in Table 9.

Table 9: Source Follower Gain and 3dB Results

	HSPICE	Chip A	Chip D
Max Gain (dB)	-1.8	-3.45	-2.87
%Diff from HSPICE	-	91.7	59.4
3dB Frequency (MHz)	47.4	6.37	6.94
%Diff from HSPICE	-	86.6	86.0

Differential Pair

No results were obtained in the laboratory as no current could be produced at the output. The HSPICE results of the DC sweeps of VINNEG are shown in Figure 28. The AC gain plot is in Figure 29. The 3dB frequency and max gain are shown in Table 10.

Table 10: Differential Pair Gain and 3dB Results

	HSPICE
Max Gain (dB)	40
3dB Frequency (MHz)	0.105

Two Stage Operational Amplifier

All tests were performed successfully in both the laboratory and in HSPICE. The results from HSPICE are plotted against the results from the chips (B and D) that produced valid results. The DC plot of OPIN vs. OPOUT is in Figure 30 and the AC gain plot is in Figure 31. The 3dB frequencies and max gains are shown in Table 11.

Table 11: Two Stage Amplifier Gain and 3dB Results

	HSPICE	Chip A	Chip D
Max Gain(dB)	64.4	76.1	75.27
%Diff from HSPICE	-	18.2%	16.9%
3dB Frequency (kHz)	11.7	1.46	1.45
%Diff from HSPICE	-	87.5%	87.6%

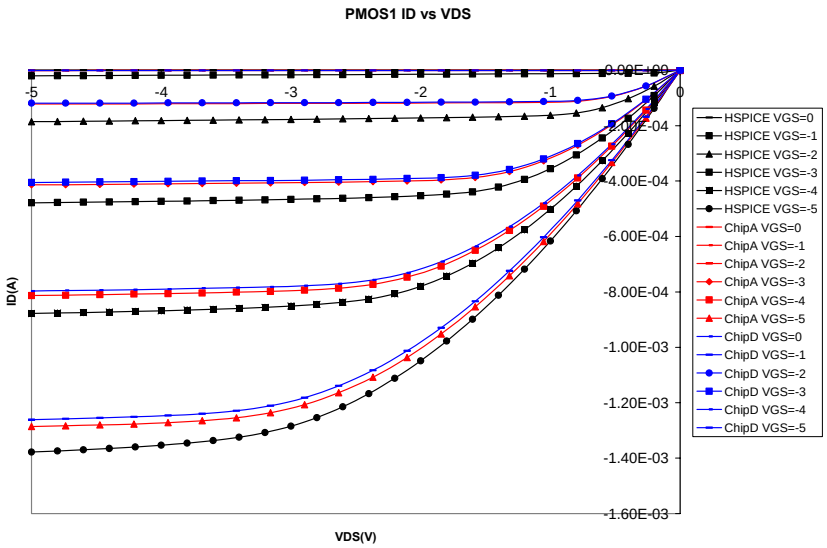

Figure 14: PMOS1-Output Characteristics ID vs. VDS

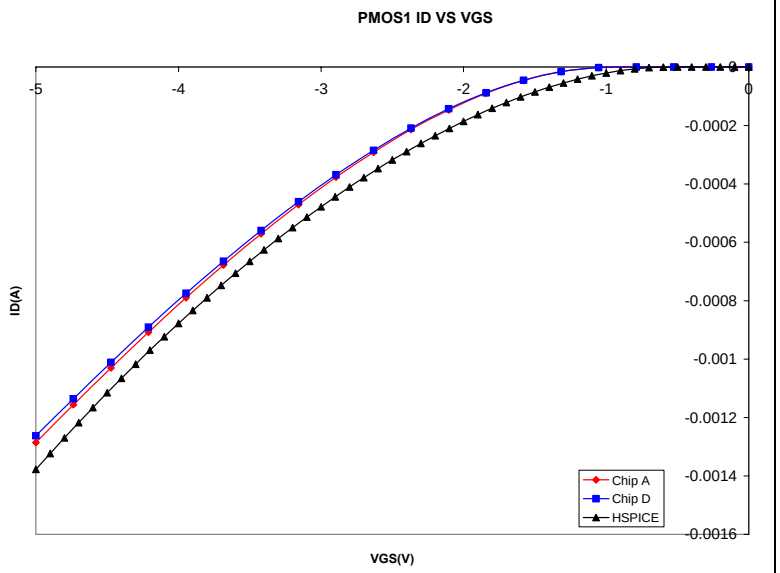

Figure 15: PMOS1- ID vs. VGS

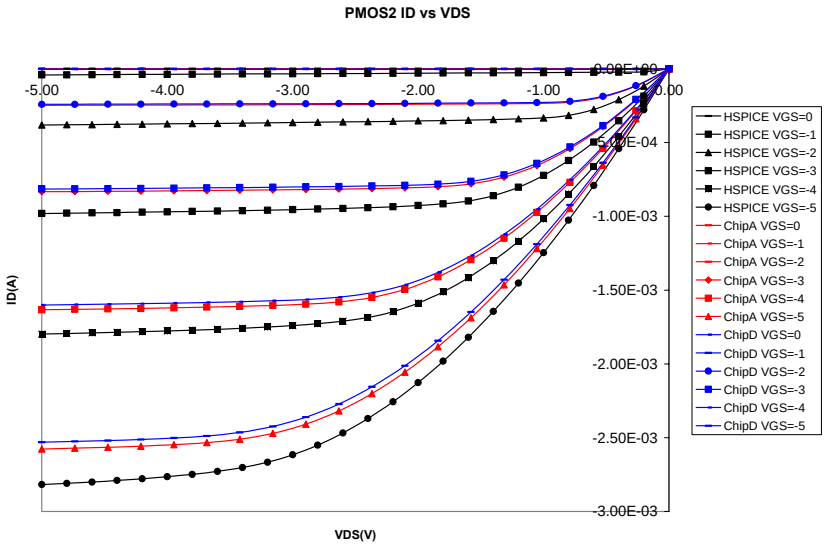

Figure 16: PMOS2-Output Characteristics ID vs. VDS

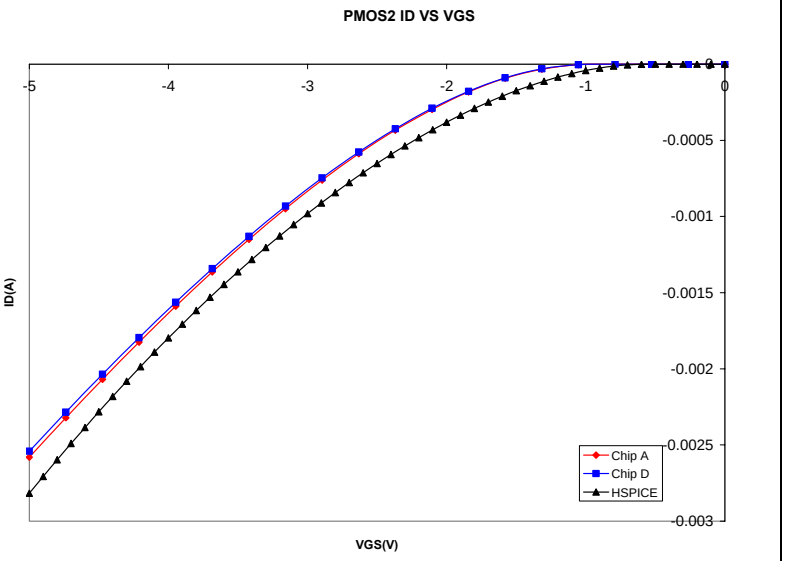

Figure 17: PMOS2- ID vs. VGS

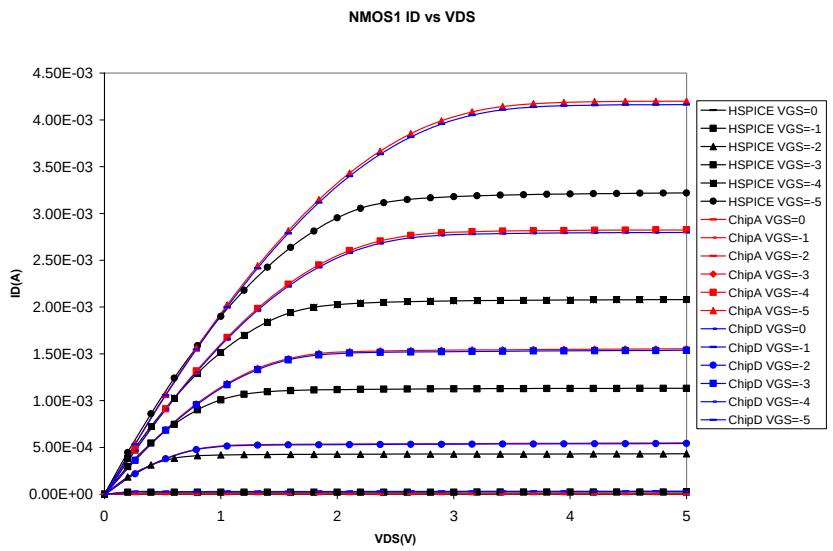

Figure 18: NMOS1-Output Characteristics ID vs. VDS

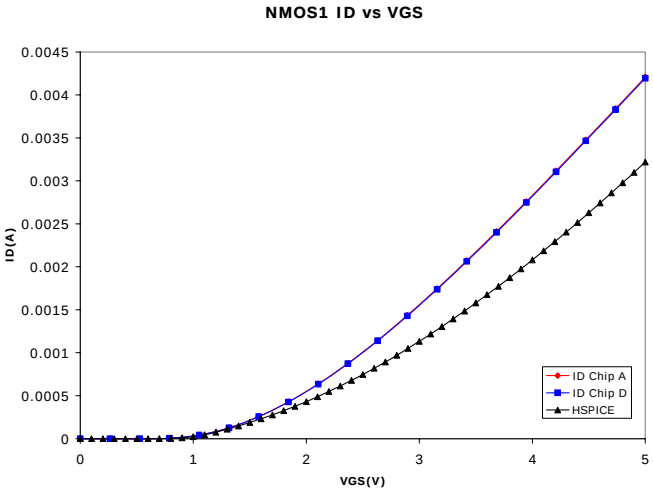

Figure 19: NMOS1- ID vs. VGS

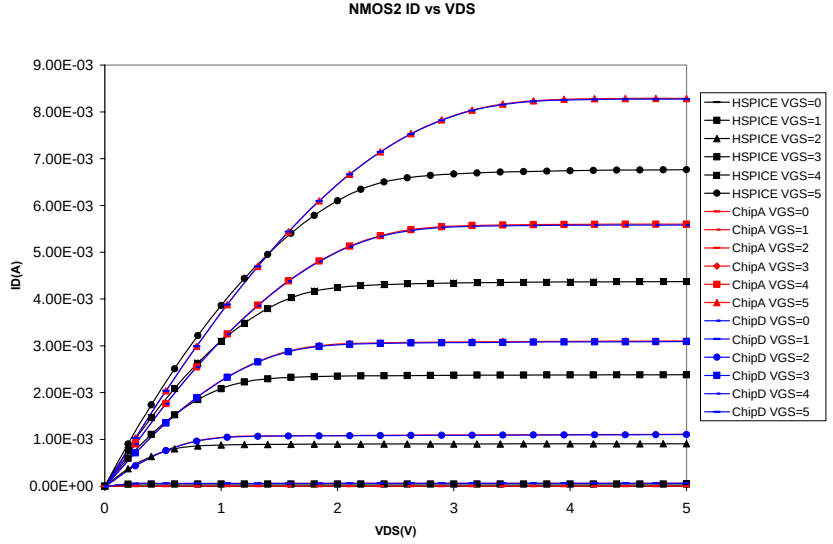

Figure 20: NMOS2-Output Characteristics ID vs. VDS

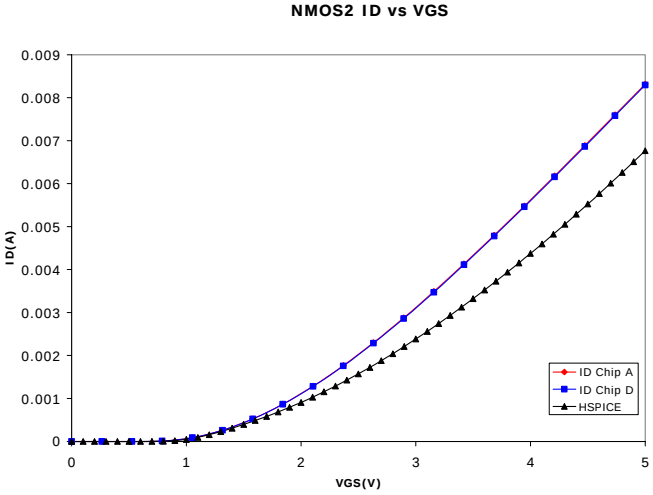

Figure 21: NMOS2- ID vs. VGS

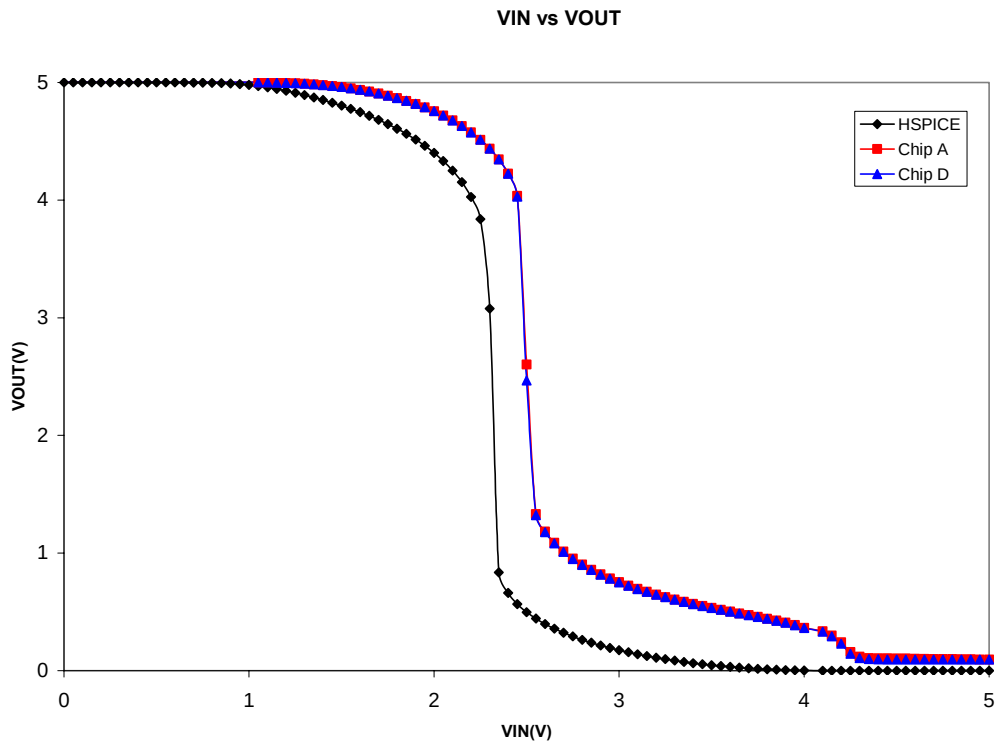

Figure 22: Inverter VIN vs. VOUT

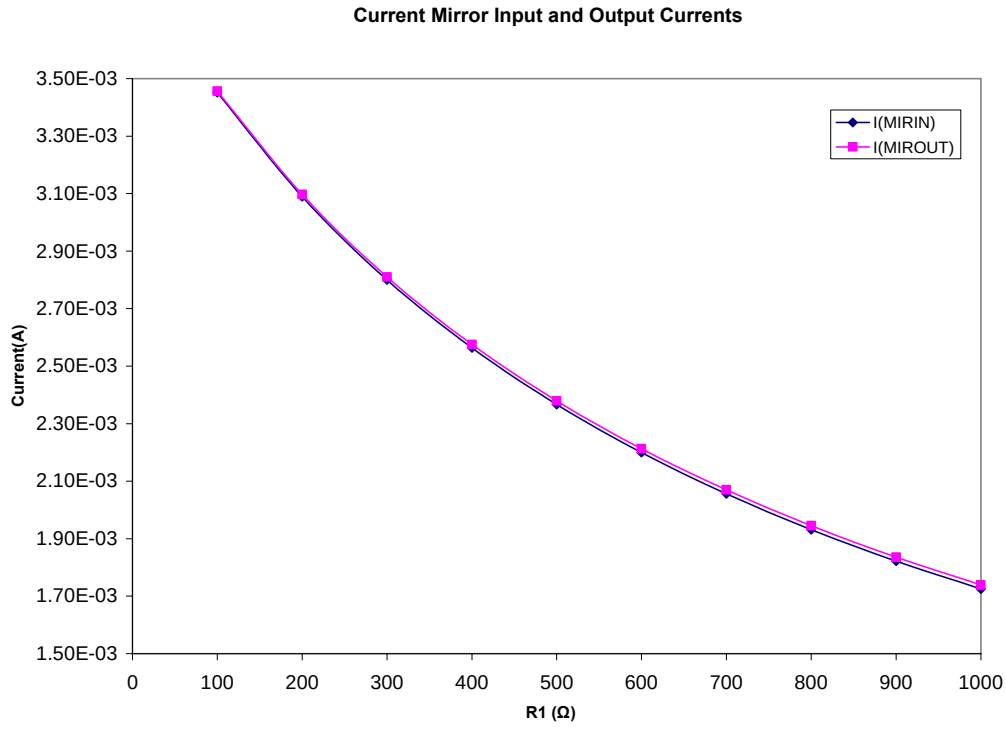

Figure23: HSPICE Current Mirror Currents

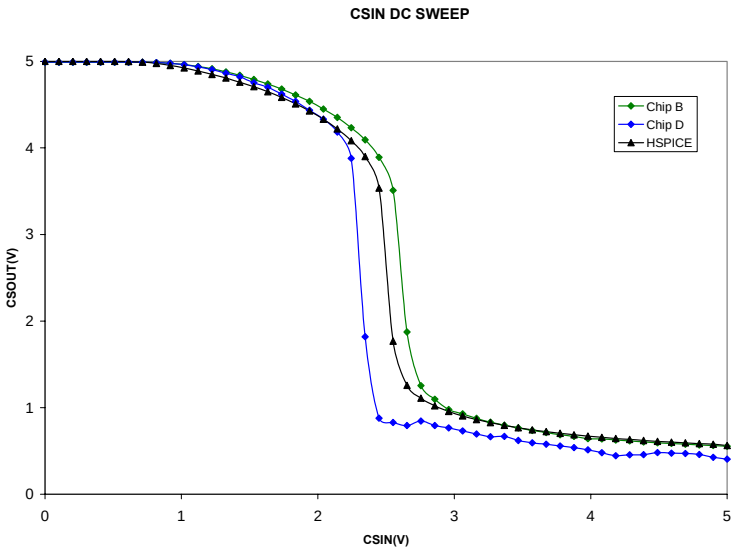

Figure 24: Common Source Amplifier DC Sweep

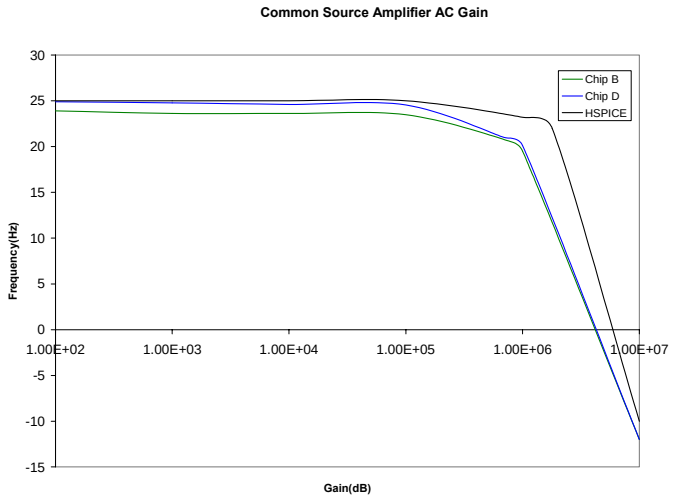

Figure 25: Common Source Amplifier AC Gain

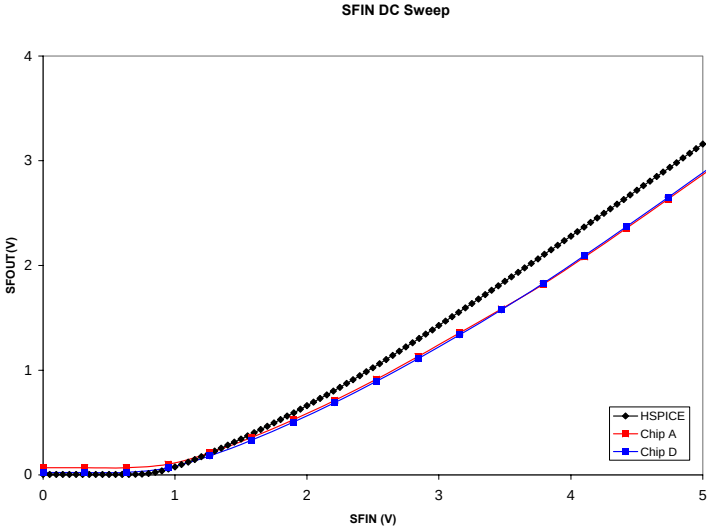

Figure 26: Source Follower DC Sweep

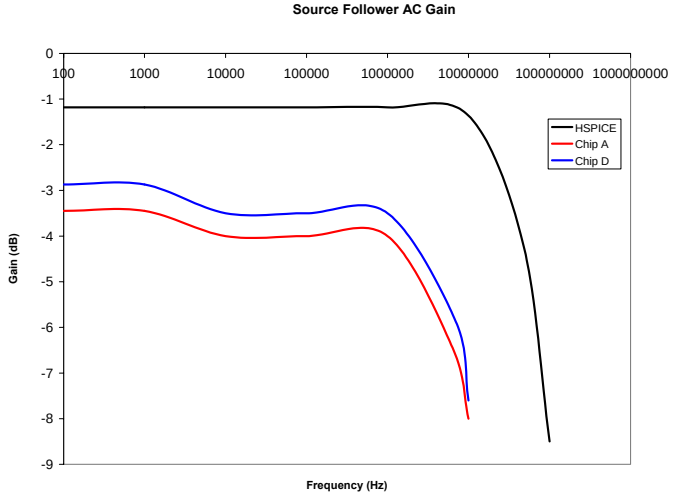

Figure 27: Source Follower AC Gain

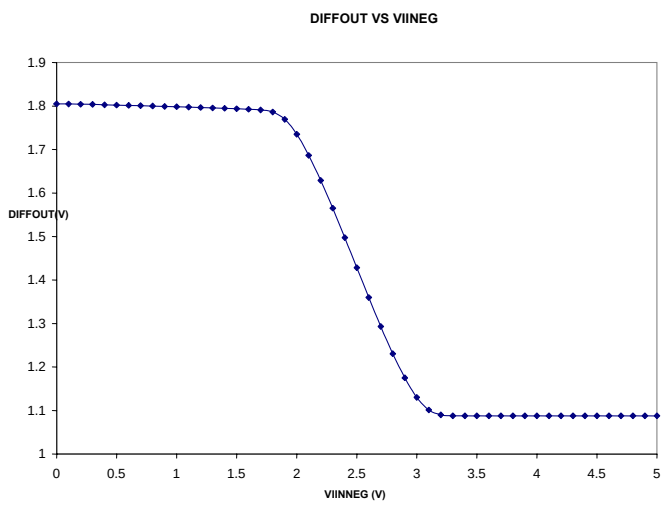

Figure 28: DiffOut vs. VINNEG

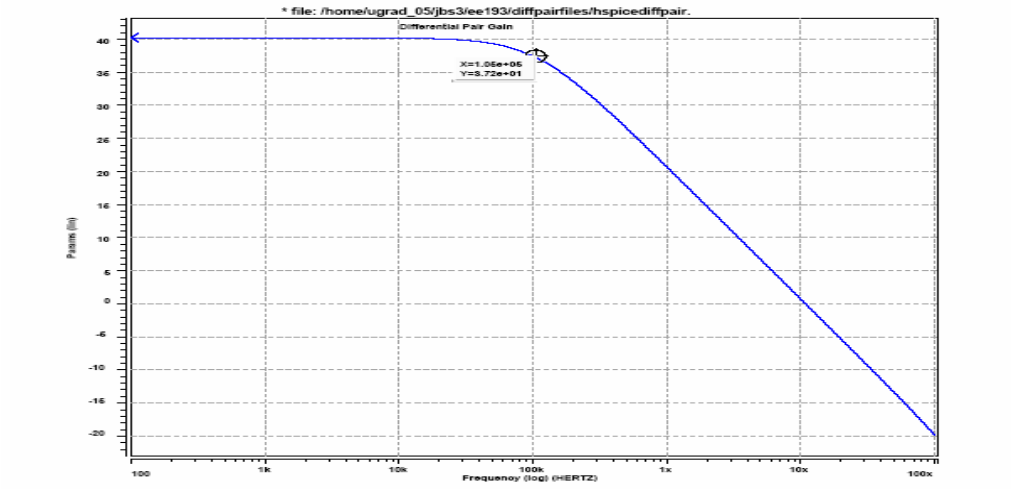

Figure 29:Diffpair AC Gain

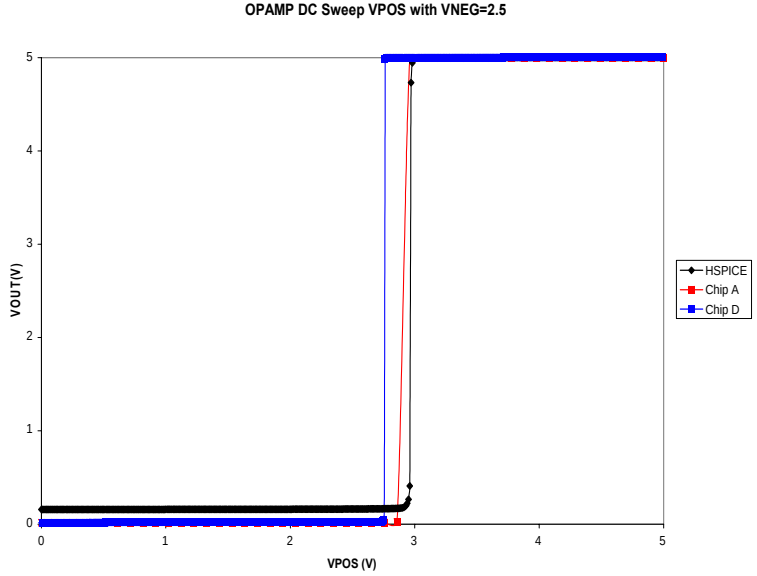

Figure 30: OPAMP DC Sweep

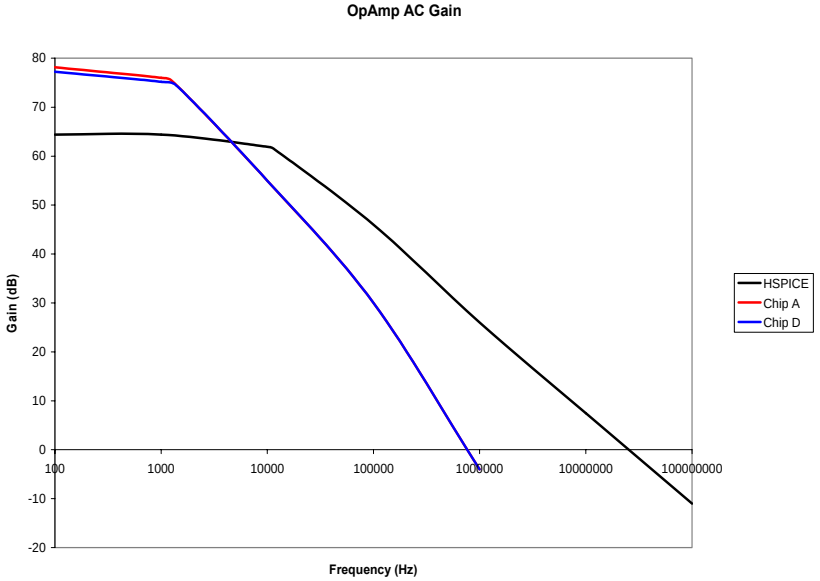

Figure 31: OPAMP AC Gain

Discussion

Each subcircuit will be discussed separately, and then there will be a summary of the overall results and issues faced while testing of the chips.

PMOS

Both HSPICE and the laboratory tests produced curves that were of the correct shape. The magnitude of the currents in the HSPICE measurements was slightly higher (~0.0005A) than the laboratory results for PMOS1 after -1V VGS. Once again for PMSO2, the magnitude of the HSPICE measurements was slightly higher (~0.0005A) than the laboratory results after -1V VGS. In both of these tests the two chips had very similar results. The currents were about twice as large in PMOS2 as compared with PMOS1 as would be expected since the width of PMOS2 is twice the width of PMOS1.

NMOS

Both HSPICE and the laboratory tests produced curves that were of the correct shape. The currents in the laboratory measurements were slightly higher (~0.001A) than the HSPICE results for NMOS1 after 1V VGS. Again with NMOS2 the actual chip measurements were higher (~0.001A) than the HSPICE simulation after 1V VGS. In both of these tests the two chips had very similar results. Also, the currents were about twice as large in the NMOS2 as compared with NMOS1 as would be expected since the width of NMOS2 is twice the width of NMOS1.

The variation within the individual device simulation and testing results could have occurred for a variety of reasons. One explanation is that the manufacturing process tends to have some variation, and so the devices will not be built exactly to specification. Another is that Spice level 49 is only a model of the actual circuit and can not perfectly model what is going to happen. These reasons can account for some of the variation present in the measurements of other subcircuits.. Since variations exist in the simplest devices, it is expected that there will be even more disparity among more complex devices.

Inverter

Chip A and D's results from HSPICE and laboratory were compared. These were the only chips with valid results. The data collected from lab and HSPICE were very similar with the main differences arising when the inverter switched from on to off. There was a slight range of approximately 0.2V for VIN where the difference between the HSPICE simulation and the laboratory results was greater than 1V. Over the range of 2.3V to 2.5V, the HSPICE results made a steep decline to low voltages, while the chips lagged slightly behind making the biggest jump at 2.55V. The two chips had very similar results. Another interesting laboratory result is that for values below 1V, both of the chips continued to slowly decline instead of jumping straight to 0V.

Current Mirror

None of the chips were able to produce valid measurements. This device seemed like it should have been easy to test, but even its simple circuit did not work properly. Measurements could only be made at MIRIN and MIROUT, so the current dissipation was unable to be traced within

the circuit in order to detect what was dysfunctional. The results from HSPICE show that the simulated version had currents at both of the outputs, which were matched even when the resistor values were not matched.

Common Source Amplifier

The DC sweep results for the common source amplifier show that the simulated results lie in between the results from the two laboratory sweeps. All of the results have the same shaped curve. When CSIN was set to 2.3V in lab and 2.5V in HSPICE, Chip D had a CSOUT of 2.5V. With Chip B when CSIN was set to 2.6V in lab and 2.5V in HSPICE, Chip B had a CSOUT of 2.5V. This demonstrates that a slight variation could be expected from chip to chip so that when gain measurements are made the proper CSIN should be chosen for the individual chip to give an output value of around 2.5V. This is especially important since the chips operate over a very narrow range.

The AC simulations also all had the same general shape, and in this case the two laboratory devices once again demonstrated that they were not perfectly matched. The maximum gain on the common source amplifier was fairly similar in HSPICE and in the laboratory, with the percent differences for the measurements in lab to the simulated results being 5.6 for Chip D and 4.9 for Chip B. The 3dB frequencies had more variation between simulation and lab with Chip B's being 57.4% different from HSPICE while Chip D varied by 61%. In contrast, the frequencies of Chips B and D were very similar in the laboratory.

The following equation is the gain equation for a Common Source Amplifier:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m (r_{ds1} \parallel r_{ds2})$$

All of the gain values were in the expected range that one would expect for this amplifier.

Source Follower

The DC sweep results for the source follower show that the simulated results are very similar to the laboratory measurements. The simulated results are slightly higher than the results from Chips A and D, which are almost perfectly matched.

For the AC gain in the laboratory it was impossible to get an output value at VDD/2, when using Figure 9. This might have been part of the reason why such a significant difference between the simulated results and the laboratory results was obtained for the gain results. This also might account for the odd shape in the gain curves.

The maximum gain on the source follower in laboratory was significantly less than the gain in HSPICE. The percent differences for the measurements in lab to the simulated results were 92% for Chip A and 59.4% for Chip D. These laboratory values were not very similar to each other as is apparent by the amount they differed from the gain in HSPICE. The 3dB frequencies also had a lot of variation with Chip A's being 86.6% different from HSPICE while Chip D's was

85.4% different. The two laboratory measurements did have fairly similar 2dB frequencies even though there was the significant difference in their maximum gains.

The following equation is the gain equation for a Source Follower.

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}$$

As is expected an ideal gain of 1 was not obtainable, but instead it was slightly less. The gain values fell within the expected range that one would expect for a source follower.

Differential Pair

The differential pair did not work in the lab. A few different setups were tested in order to try to obtain a signal at the output, but none of the test circuits worked. Again as with the current mirror only the input and output signals could be measured so the dissipation of current inside of the circuit could not be traced. The simulated results were normal.

Two Stage Operational Amplifier

The results from the DC sweep were all very similar. The simulated results rose from 0 to 5V between 2.96V and 2.97V. The output rose from 0 to 5V between 2.86V and 2.87V for chip A. The output rose from 0 to 5V between 2.75V and 2.76V for chip D. These results show that there is a slight offset voltage as input to VINNEG was 2.5V for these results. The data also shows how large the gain was for each of these devices.

A special circuit had to be used to measure the gain as the gain was so steep across such a narrow range. This meant that the feedback circuit in Figure 12 was used to help stabilize the output. The two lab plots were very noisy below frequencies of 1 kHz. In this case both of the laboratory gains were 76.1dB for Chip A and 75.27dB for Chip D, which were both significantly higher than the 64.4db gain simulated in HSPICE. The 3dB frequency was 1.46 kHz for Chip A, 1.45 kHz for Chip D, and 11.7 kHz for HSPICE. The two chips that produced results had very similar data, but they were not that close in comparison to the HSPICE results at low frequencies. After the 3dB frequency they all tended to follow a similar trend.

Problems Encountered

The most significant problem encountered was the fact that two of the devices tested failed to work on any of the chips. These two devices, the current mirror and the differential pair, both worked in simulation; but in the laboratory no current could ever be produced at these devices' outputs. The devices were set up with external contacts only on their inputs and outputs, making it impossible with the equipment available in lab to test the values inside of the devices and see where the current was going.

Another problem encountered was that the operating range on many of the devices was very narrow. On the operational amplifier a special circuit had to be used for testing to get the output to sit at VDD/2.

In every gain plot the HSPICE results had a higher 3dB frequency than the values obtained in the laboratory. This might have been due to the fact that the capacitances could not be perfectly measured in the devices used in lab, and because the HSPICE model is not a perfect representation of the actual device. In most cases the 3dB frequency was off by about one order of magnitude. The common source amplifier had the best matched gain results with the maximum magnitudes of the simulation close to the measured results. The source follower and the op amp had variations between measured and simulated with the simulated chip having a higher maximum gain for the source follower and a lower maximum gain for the op amp.

The last major problem encountered was the low yield of the packaged chips. While five chips were available for testing, two of the chips never produced any results. Chips A, B, and D worked for some of the devices, but none of them worked for all of the devices tested. Since this test is designed to be used in a laboratory setting, a higher yield is desirable. This low yield would mean that 2/5 of the packaged chips could be expected to not work.

Future Work

The current chip does not seem reliable enough to serve its purpose as a means to study CMOS technology in the Electrical Engineering lab. The chip could be improved by repackaging it with another company in order to see if both the yield and laboratory results can be improved. Also, what would probably be most useful would be to reproduce the chips. Currently the chips include many more complex devices that are not necessary in an introductory course. These devices could be removed, and more test pins to internal nodes could be added to allow the devices to be tested more easily. Additionally, several basic logic gates could be added as these devices would also be useful in an introductory course.

Conclusion

The main conclusion drawn from this study is that the chips are unable to fulfill the needs of the Electrical Engineering department. The chips are too unreliable, some of the individual devices were never functional, and many of the packaged chips did not even work. Only one of the chips, Chip D, had fully functional subcircuits, aside from its current mirror and differential pair. Chips A and B only had some functional subcircuits. The chip results tended to be fairly similar,

but there was not enough consistency in their functionality. Generally, a high level of correlation existed between the DC testing and simulation results. The AC results tended to exhibit more variation, but still fell within an expected range. The laboratory manual was not produced because Drs. Derby and Morizio decided that more work was needed on the chips before they could be used in the laboratory.